Amendments to the Claims

1. (Currently Amended) A driving method for displaying a normal mode signal in a wide mode liquid crystal display (LCD) device, for displaying an analog video signal having a horizontal back porch input to the wide mode LCD device as a normal mode, the method comprising:

outputting a source start pulse (SSP) signal;

latching pixel data for a black display by using a main clock signal having a ~~short~~ first period synchronized to the SSP signal;

first skipping data latch during a first transition period of the video signal;

latching pixel data corresponding to a normal mode by using a modulated clock signal having a second ~~long~~ period that is longer than the first period, and outputting the latched pixel data; and

second skipping data latch during a second transition period of the video signal.

2. (Original) The driving method of claim 1, wherein in the outputting step, the SSP signal is output after a predetermined time period from a horizontal start pulse (HSP).

3. (Original) The driving method of claim 2, wherein the predetermined time period is 1.048μs.

4. (Original) The driving method of claim 2, wherein in the outputting step, the SSP

signal is output after a certain time period from a rising edge of the HSP.

5. (Original) The driving method of claim 1, wherein in the first skipping step, the data latch corresponding to 42 to 45 pixels is skipped.

6. (Original) The driving method of claim 1, wherein in the second skipping step, the data latch corresponding to 52 pixels is skipped.

7. (Currently Amended) The driving method of claim 1, wherein the ~~short~~ first period of the clock signal lasts from a start of the SSP signal to an end of ~~a~~ the horizontal back porch ~~of the clock signal~~.

8. (Original) The driving method of claim 1, wherein at least one of the first and second skipping steps is performed by disenabling an enable clock signal.

9. (Original) The driving method of claim 1, wherein the long period of the clock signal corresponds to 50.3μs.

10. (Currently Amended) A method for displaying a video signal having a horizontal back porch in a display device, comprising:

generating a source start pulse signal;

latching pixel data for a black display from a start of the source start pulse signal to an end of ~~a~~ the horizontal back porch ~~of a clock signal~~; and

skipping latch of subsequent pixel data during a transition period of the video signal.

11. (Original) The method of claim 10, further comprising:

latching subsequent pixel data during a high-level of the video signal; and

skipping latch of subsequent pixel data during a second transition period of the video signal.

12. (Original) The method of claim 10, wherein in the generating step, the source start pulse signal is output after a predetermined time period from a horizontal start pulse (HSP).

13. (Original) The method of claim 12, wherein in the generating step, the predetermined time period is 1.048μs.

14. (Original) The method of claim 10, wherein in the skipping step, the latch of 42 to 45 pixels of data is skipped.

15. (Currently Amended) The method of claim 10, wherein in the latching step, the start of the source start pulse signal to the end of the horizontal back porch ~~of the clock signal~~ is about 3.14μs.

16. (Currently Amended) A driving device for displaying a video signal having a horizontal back porch in a display device, comprising:

means for generating a source start pulse signal;

means for latching pixel data for a black display from a start of the source start pulse signal to an end of a the horizontal back porch ~~of a clock signal~~; and

means for skipping latch of subsequent pixel data during a transition period of the video signal.

17. (Original) The driving device of claim 16, further comprising:

means for latching subsequent pixel data during a high-level of the video signal; and

means for skipping latch of subsequent pixel data during a second transition period of the video signal.

18. (Original) The driving device of claim 16, wherein the source start pulse signal is output after a predetermined time period from a horizontal start pulse (HSP).

19. (Original) The driving device of claim 18, wherein the predetermined time period is 1.048μs.

20. (Original) The driving device of claim 16, wherein the skipping means skips the latch of 42 to 45 pixels of data.

21. (Currently Amended) The driving device of claim 16, wherein the start of the source start pulse signal to the end of the horizontal back porch ~~of the clock signal~~ is about 3.14μs.